Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

Claim 1 (Canceled)

Claim 2 (Previously presented): An apparatus for exercising semiconductor devices, said apparatus comprising:

a plurality of semiconductor devices, each comprising a plurality of elongate, spring connection elements;

a support substrate comprising a plurality of terminals;

test connection means for connecting said terminals to a test device;

a plurality of socket substrates disposed on said support substrate, each said socket comprising a plurality of sockets and a plurality of traces, each said trace electrically connected to one of said sockets;

means for electrically connecting ones of said traces with ones of said terminals; and

means for pressing ones of said spring connection elements against ones of said sockets, wherein said spring connection elements generate spring counterforces and thereby form pressure connections with said sockets.

Claim 3 (Previously presented): The apparatus of claim 2, wherein said plurality of semiconductor devices are dies of an unsingulated semiconductor wafer.

Claim 4 (Currently amended): The apparatus of claim 3, wherein each socket substrate corresponds to one ~~die~~ of said dies.

Claim 5 (Previously presented): The apparatus of claim 3, wherein said support substrate is part of a probe card assembly.

Claim 6 (Previously presented): The apparatus of claim 5, wherein said support substrate is electrically connected through an interposer to a probe card, and wherein said support substrate, said interposer, and said probe card compose said probe card assembly.

Claim 7 (Previously presented): The apparatus of claim 2, wherein said semiconductor devices are unpackaged, singulated semiconductor dies.

Claim 8 (Previously presented): The apparatus of claim 2, wherein said test device provides test signals to test a functionality of said semiconductor devices.

Claim 9 (Previously presented): The apparatus of claim 2, wherein said test device provides power to said semiconductor devices, and further comprising a temperature control device disposed to control a temperature of said semiconductor devices.

Claim 10 (Previously presented): The apparatus of claim 9, wherein said temperature control device comprises:

a first thermal chuck in thermal contact with said semiconductor devices; and

a second thermal chuck in thermal connect with said socket substrates.

Claim 11 (Previously presented): The apparatus of claim 2, wherein said socket substrates are disposed in rows on said support substrate, and further comprising a plurality of power lines disposed on said support substrate, each said power line corresponding to one of said rows of socket substrates and supplying power to every socket substrate in said row.

Claim 12 (Previously presented): The apparatus of claim 11, further comprising a plurality of isolation resistors, each said isolation resistor disposed between one of said power lines and one of said socket substrates.

Claim 13 (Previously presented): The apparatus of claim 2, wherein said means for securing comprises one of a test head or a vacuum chuck.

Claim 14 (Previously presented): The apparatus of claim 2, wherein said means for electrically connecting ones of said traces with ones of said terminals comprise a plurality of bond wires, each said bond wire bonded to one of said traces and to one of said terminals.

Claim 15 (Previously presented): The apparatus of claim 2, wherein said sockets comprise pits etched into a surface of a corresponding socket substrate.

Claim 16 (Previously presented): The apparatus of claim 2, wherein said socket substrate comprises silicon.

Claim 17 (Currently amended): A test socket apparatus comprising:

a support substrate comprising a plurality of terminals;

test connection means for connecting said terminals to a test device;

a socket substrate disposed on said support substrate and comprising a plurality of sockets and a plurality of traces, each said trace electrically connected to one of said sockets;

means for electrically connecting ones of said traces with ones of said terminals; and

means for pressing elongate spring connection elements disposed on ~~said~~ a semiconductor device against said sockets such that said spring connection elements generate spring counterforces and thereby form pressure connections with said sockets.

Claim 18 (Previously presented): The apparatus of claim 17, wherein said test device provides test signals to test a functionality of said semiconductor device.

Claim 19 (Previously presented): The apparatus of claim 17, wherein said test device provides power to said semiconductor device, and further comprising thermal means for controlling a temperature of said semiconductor device.

Claim 20 (Previously presented): The apparatus of claim 17, wherein said means for electrically connecting ones of said traces with ones of said terminals comprise a plurality of bond wires, each said bond wire bonded to one of said traces and to one of said terminals.

Claim 21 (Previously presented): The apparatus of claim 17, wherein said sockets comprise pits etched into a surface of said socket substrate.

Claim 22 (Previously presented): The apparatus of claim 17, wherein said socket substrate comprises silicon.

Claim 23 (Previously presented): The apparatus of claim 17 further comprising a plurality of said socket substrates.

Claims 24-36 (Cancelled)

Claim 37 (New): The apparatus of claim 2, wherein the plurality of elongate, spring connection elements have a pitch off less than about 5 mils.

Claim 38 (New): The apparatus of claim 17, wherein the elongate spring connection elements have a pitch of less than about 5 mils.